CLAIMS

What is claimed is:

1. A method for improving an input match in a circuit comprising:

operating a cascode having an input signal port with an input signal impedance and further having a stage gain controlled by a level setting gain control voltage;

and

operating an impedance compensating circuit for changing a compensating impedance presented at the input signal port,

wherein the impedance compensating circuit is controlled by the level setting gain control voltage and wherein the impedance compensating circuit is operable to counteract changes in the input signal impedance correlated with changes in the stage gain.

2. The method of claim 1 wherein:

the impedance compensating circuit is connected in parallel with the input signal port.

3. The method of claim 1 wherein:

the impedance compensating circuit is connected in series with the input signal port.

4. The method of claim 1 wherein:

the impedance compensating circuit is connected in series-parallel with the input signal port.

5. The method of claim 1 wherein:

the cascode is implemented using Gallium Arsenide transistors.

6. The method of claim 1 wherein:

the cascode is implemented using metal-oxide semiconductor transistors formed as an integrated circuit.

7. The method of claim 1 wherein:

the cascode is implemented using devices selected from a list consisting of metal-oxide semiconductor transistors, silicon bipolar transistors and germanium transistors.

8. A circuit for processing a signal comprising:

a cascode having

a first transistor connected in a configuration selected from a group consisting of a common gate configuration and a common base configuration

and

a second transistor connected in a configuration selected from a group consisting of a common source configuration, a common drain configuration, a common emitter configuration and a common collector configuration;

a gain controller operable to adjust a gain of the cascode in response to a control signal; and

an impedance controller operable to adjust an input impedance of the cascode with a loading impedance in response to the control signal;

whereby the circuit operates with input impedance compensation.

9. The circuit of claim 8 wherein

the circuit is an amplifier.

10. The circuit of claim 8 wherein

the circuit is an amplifier that operates at a narrow band of frequencies in the microwave region.

11. The circuit of claim 8 wherein

the circuit is implemented as a single integrated circuit.

12. The circuit of claim 8 wherein

the circuit is implemented using metal-oxide semiconductor technologies.

13. The circuit of claim 8 wherein

the circuit is implemented using Gallium Arsenide technologies.

14. The circuit of claim 8 wherein

the impedance controller comprises an inverter.

15. The circuit of claim 8 wherein

the gain controller outputs a DC bias voltage that is applied to a control terminal of the first transistor.

16. A circuit for processing a signal comprising:

a cascode having

a first transistor connected in a configuration selected from a group consisting of a common gate configuration and a common base configuration

and

a second transistor connected in a configuration selected from a group consisting of a common source configuration, a common drain configuration, a common emitter configuration and a common collector configuration;

a controller operable to adjust a gain of the cascode in response to a control signal and further operable to adjust an input impedance of the cascode with a loading impedance in response to the control signal;

whereby the circuit operates with input impedance compensation.

17. The circuit of claim 16 wherein

the circuit is an amplifier that operates at a narrow band of frequencies in the microwave region.

18. The circuit of claim 16 wherein

the circuit is implemented as a single integrated circuit.

19. The circuit of claim 16 wherein

the circuit is implemented using metal-oxide semiconductor technologies.

20. The circuit of claim 16 wherein

the circuit is implemented using Gallium Arsenide technologies.